CLAIMS

What is claimed is:

1. A content addressable memory (CAM) cell comprising:

four storage elements; and

four switching circuits each coupled between a first match line and a reference node, each of the switching circuits having a first input coupled to a respective one of the four storage elements, and a second input coupled to a respective one of four compare lines.

2. The CAM cell of claim 1 wherein, during a compare operation, the four switching circuits receive a four-bit comparand value from the four compare lines, the four-bit comparand value including three bits in a first state and one bit in a second state.

3. The CAM cell of claim 1 wherein at least one of the switching circuits comprises first and second transistors coupled in series between the first match line and the reference node, the first and second transistors having respective control terminals that constitute the first input and the second input of the at least one of the switching circuits.

4. The CAM cell of claim 1 wherein the control terminals are gate terminals.

5. The CAM cell of claim 1 wherein each of the switching circuits is a logic AND gate.

6. The CAM cell of claim 1 further comprising four additional switching circuits each coupled between a second match line and the reference node, and each having a first input coupled to a respective one of the four storage elements, and a second input coupled to a

respective one of four additional compare lines.

7. The CAM cell of claim 1 wherein the reference node is a ground reference node.

8. The CAM cell of claim 1 wherein each of the storage elements is a static storage element.

9. The CAM cell of claim 1 wherein each of the storage elements is a dynamic storage element.

10. The CAM cell of claim 1 wherein each of the storage elements is a nonvolatile storage element.

11. The CAM cell of claim 1 further comprising four pairs of access transistors, each pair of access transistors being coupled between a respective one of the four storage elements and a respective one of four pairs of bit lines.

12. The CAM cell of claim 11 wherein the four pairs of access transistors each have a control terminal coupled in common to a first word line.

13. The CAM cell of claim 1 further comprising a first access transistor coupled between a first one of the four storage elements and a first bit line, a second access transistor coupled between the first one of the four storage elements and a second bit line, a third access transistor coupled between a second one of the four storage elements and the first bit line, and a fourth access transistor coupled between the second one of the four storage elements and the second bit line.

14. The CAM cell of claim 1 wherein the first and second access transistors have respective

control terminals coupled to a first word line, and the third and fourth access transistors have respective control terminals coupled to a second word line.

15. The CAM cell of claim 1 wherein the first input of each of the four switching circuits is coupled to an inverting output of the respective one of the four storage elements.

16. A content addressable memory (CAM) device comprising:
a plurality of columns of CAM cells; and
a plurality of decoder circuits to decode respective groups of bits of a comparand value into corresponding sets of decoded signals, and coupled to provide each of the sets of decoded signals to a respective one of the columns of CAM cells.

17. The CAM device of claim 16 wherein each group of bits includes M constituent bits and each corresponding set of decoded signals includes N constituent signals, N being greater than M.

18. The CAM device of claim 17 wherein $N = 2^M$.

19. The CAM device of claim 16 wherein each of the groups of bits of the comparand value includes two constituent bits and each corresponding set of decoded signals includes four constituent signals.

20. The CAM device of claim 16 wherein each of the plurality of decoder circuits decodes the respective group of bits of the comparand value into the corresponding set of decoded signals such that one signal of the set of decoded signals has a first state and the remaining signals of the set of decoded signals have a second state.

21. The CAM device of claim 20 wherein the one signal having the first state is a first, second, third or fourth one of the decoded signals according to whether the corresponding group of bits of the comparand value have a first, second, third or fourth state, respectively.

22. The CAM device of claim 16 further comprising a plurality of mapping sub-circuits to convert respective groups of bits of a write data value into corresponding sets of data state signals, the mapping sub-circuits being coupled to provide the sets of data state signals to the columns of CAM cells, respectively.

23. The CAM device of claim 22 wherein the write data value comprises:
a data word having constituent data bits; and
a mask word having constituent mask bits, and wherein the each of the mapping sub-circuits is configured to convert a respective group of the data bits and a respective group of the mask bits into the corresponding set of data state signals.

24. The CAM device of claim 22 wherein each of the sets of data state signals is a set of complementary signals.

25. The CAM device of claim 22 wherein each of the sets of data state signals includes N signals in a first state and M minus N signals in a second state, N ranging from one to M and being the number of permutations of a first group of bits of a comparand value that match a corresponding one of the groups of bits of the write data value.

26. The CAM device of claim 25 wherein the number of permutations of the first group of bits of a comparand value that match the corresponding one of the groups of bits of the write

data value is one (1) if no mask bits included within the corresponding one of the groups of bits of the write data value indicate a mask condition.

27. The CAM device of claim 25 wherein the number of permutations of the first group of bits of a comparand value that match the corresponding one of the groups of bits of the write data value is 2^R, R being the number of mask bits included within the corresponding one of the groups of bits of the write data value that indicate a mask condition.

28. A content addressable memory (CAM) device comprising:

an array of CAM cells;

a write mapping circuit to convert an input data word into a converted data word having one of at least two different patterns of constituent bits according to the state of a first control signal; and

a read/write circuit coupled to receive the converted data word from the write mapping circuit and coupled to the array of CAM cells to output the converted data word thereto.

29. The CAM device of claim 28 wherein the two different patterns of bits comprise equal numbers of bits.

30. The CAM device of claim 28 wherein the input data word includes data bits and mask bits with each of the data bits and mask bits constituting a respective data/mask bit pair, and wherein each set of four bits within the converted data word includes 2^R bits in a first state and the remaining bits in a second state if the first control signal selects a first conversion mode, R being the number of mask bits in a masking state within a group of two data/mask

bit pairs.

31. The CAM device of claim 30 wherein each set of four bits within the converted data word includes R-2 bits in a first state and the remaining bits in a second state if the first control signal selects a second conversion mode.

32. The CAM device of claim 31 wherein the converted data word is complemented prior to being stored within the array of CAM cells if the first control signal selects the second conversion mode.

33. The CAM device of claim 30 wherein the converted data word is complemented prior to being stored within the array of CAM cells if the first control signal selects the first conversion mode.

34. The CAM device of claim 28 further comprising a write data selector having a first input port coupled to receive the converted data word from the write mapping circuit and a second input port coupled to receive the input data word, the write data selector being responsive to a second control signal to output either the converted data word or the input data word to the read/write circuit.

35. The CAM device of claim 28 further comprising a read mapping circuit coupled to receive a read data word from the read/write circuit and configured to convert the read data word into a converted data word having one of at least two different patterns of constituent bits according to the state of the first control signal.

36. A method of operation within a content addressable memory (CAM) device, the method

comprising:

decoding respective pairs of bits within a comparand value into corresponding four-bit map values in which one bit is in a first state and the remaining three bits are in a second state; and

outputting each of the map values onto a respective set of four compare lines within the CAM device.

37. The method of claim 36 further comprising storing the comparand value in a comparand register prior to decoding the respective pairs of bits.

38. The method of claim 36 further comprising storing the map values in a comparand register prior to outputting the map values onto respective sets of compare lines.

39. The method of claim 36 further comprising selecting either a first operating mode or a second operating mode within the CAM device, and wherein decoding respective pairs of bits within a comparand value into corresponding four-bit map values comprises decoding the respective pairs of bits within the comparand value into corresponding four-bit map values if the first operating mode is selected.

40. The method of claim 39 further comprising outputting each bit of the comparand value in complementary form onto a respective pair of the compare lines within the CAM device if the second operating mode is selected.

41. A method of operation within a content addressable memory (CAM) device, the method comprising:

receiving an N-bit comparand value; and

activating less than N compare lines within the CAM device to compare each of the N bits of the comparand value with contents of CAM cells coupled to the N compare lines.

42. The method of claim 41 further comprising converting the N-bit comparand value into a 2N-bit compare word in which each group of four bits includes one bit in a first state and three bits in a second state.

43. The method of claim 42 wherein activating less than N compare lines within the CAM device comprises activating a selected compare line within each set of four compare lines, the selected compare line corresponding to the one bit in the first state.

44. The CAM device of claim 43 wherein activating the selected compare line comprises outputting a logic high signal on the selected compare line.

45. The method of claim 42 wherein converting the N-bit comparand value into a 2N-bit compare word comprises decoding each pair of bits in the comparand value into respective groups of four bits in which each group of four bits includes the one bit in the first state and the three bits in the second state.

46. The method of claim 41 further comprising:

receiving a 2N-bit write value containing N data bits and N mask bits, each of the mask bits corresponding to a respective one of the data bits to form a data/mask pair; and

converting each distinct group of four bits within the write value into a corresponding four-bit map value having 2^R bits in a first state and remaining bits in a second state, R being the number of mask bits in the distinct group of four bits within the write value that are in a masking state.

47. The method of claim 46 wherein each distinct group of four bits within the write value includes two mask bits and two data bits.

48. The method of claim 46 further comprising outputting the map value onto a set of bit lines for storage within a CAM cell within the CAM array.

49. A method of operation within a content addressable memory (CAM) device, the method comprising:

converting a four-bit write data entity containing two mask bits and two data bits into a four-bit data map value having 2^R bits in a first state, R being the number of mask bits in the write data entity that indicate a masking condition; and

providing a complement of the data map value to a compare circuit within a CAM cell.

50. The method of claim 49 further comprising:

converting a two-bit comparand entity into a four-bit comparand map value having one bit in the first state and remaining bits in a second state; and

providing the comparand map value to the compare circuit.

51. The method of claim 50 further comprising comparing the comparand map value with the complement of the data map value within the compare circuit.

52. The method of claim 51 wherein comparing the comparand map value with the complement of the data map value comprises providing the four-bits of the complement of the data map value to first inputs of respective switching circuits within the compare circuit and providing the four-bits of the comparand map value to second inputs of the respective

switching circuits.

53. The method of claim 52 wherein each of the switching circuits within the compare circuit is switched to a conducting state if the bits of the complement of the data map value and the comparand map value are both in the first state.

54. The method of claim 52 wherein each of the switching circuits are coupled between a first match line and a reference node.

55. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of columns of CAM cells;

means for decoding respective pairs of bits within a comparand value into corresponding four-bit map values in which one bit is in a first state and the remaining three bits are in a second state; and

means for outputting each of the map values to a respective one of the columns of the CAM cells.

56. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of CAM cells and 2N compare lines, N being an integer value;

means for receiving an N-bit comparand value; and

means for activating less than N of the 2N compare lines within the CAM device to compare each of the N bits of the comparand value with contents of CAM cells coupled to the 2N compare lines.

57. The CAM device of claim 56 further comprising means for converting the N-bit

comparand value into a 2N-bit compare word in which each group of four bits includes one bit in a first state and three bits in a second state.

58. The CAM device of claim 57 wherein activating less than N of the 2N compare lines comprises means for activating a selected compare line within each set of four compare lines, the selected compare line corresponding to the one bit in the first state.

59. A content addressable memory (CAM) device comprising:

a CAM cell including a storage circuit and a compare circuit;

means for converting a four-bit write data entity containing two mask bits and two data bits into a four-bit data map value having 2^R bits in a first state, R being the number of mask bits in the write data entity that indicate a masking condition; and

means for providing a complement of the data map value to the compare circuit.

60. The CAM device of claim 59 further comprising:

means for complementing the data map value to generate the complement of the data map value; and

means for storing the complement of the data map value in the storage circuit.

61. The CAM device of claim 59 further comprising means for storing the data map value in the storage circuit, and wherein the storage circuit comprises means for providing the complement of the data map value to the compare circuit.